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United States Patent [19]

Matsutani

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[54] **METHOD OF PRODUCING
INSULATED-GATE FIELD EFFECT
TRANSISTOR**

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437/44; 437/89; 148/DIG. 82[58] Field of Search 437/44, 45, 43, 89,
437/40, 913; 148/DIG. 82, DIG. 122

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[57] ABSTRACT

A polysilicon layer of approximately 500Å in thickness and a PSG layer approximately 3000Å in thickness are sequentially layered on a silicon wafer on which a gate insulating layer is formed; an opening having been formed in the PSG layer. After forming a side wall layer made of PSG of predetermined thickness in the opening, a second polysilicon layer for a leg portion of an inverse-T gate is embedded in the opening and both PSG layers are removed. Then, n⁻ impurities are doped by ion implantation by using the second polysilicon layer as a mask, forming a LDD region. Another side wall layer is formed on the second polysilicon layer, and then, the first polysilicon layer, exposed outside of the second polysilicon layer and the side wall layer, is etched. Under the side wall layer, that polysilicon layer constituting a top of the inverse-T gate remains. Ion implantation is implemented by using the second polysilicon layer and the side wall layer as masks, such that a n⁺ source and n⁺ drain are formed. Since the n⁻ impurities are doped by the ion implantation through the first polysilicon layer having an even thickness, the junction depth in the LDD region is constant. Additionally, since the thickness of the first polysilicon layer is small, the gate insulating layer reliably functions as an etch-stop in patterning the polysilicon layer.

7 Claims, 12 Drawing Sheets

